(1)

M/A-COM LINKABIT, Inc.
10453 Roselle Street
San Diego, CA 92121

QUARTERLY TECHNICAL REPORT

ON THE

EARTH STATION INTERFACE

FOR

DEMAND ASSIGNMENT APPLICATIONS

FOR THE PERIOD 1 JULY 1982 THROUGH 30 SEPTEMBER 1982

Sponsored by:

Defense Advanced Research Projects Agency

ARPA Order Number 3674/5

and

Defense Communications Agency

Contracting Agency: DSSW

Contract Number MDA903-81-C-0638

Effective Date of Contract: 81 SEP 08

Expiration Date of Contract: 83 DEC 31

JOHN E. McCORMICK
Program Manager
(714) 457-2340 X 2358

"The views and conclusions contained in this document are those of the authors and should not be interpreted as representing the official policies, either expressed or implied, of the Defense Advanced Research Projects Agency or the U. S. Government."

1. INTRODUCTION

The ESI interface with a message processor for Bolt Beranek and Newman called the PSAT. M/A-COM LINKABIT does not have a PSAT, but design verification testing must be performed in order to insure the enhancements performed under this contract meet the requirements set forth in the proposal. In addition, each of the six ESI's produced will require the performance of an Acceptance Test Procedure prior to shipment.

M/A-COM LINKABIT has proposed the design and construction of a PSAT Emulator which could exercise the ESI in a manner which approximates the PSAT well enough to verify operational status. The PSAT Emulator is designed around a Hewlett Packard 9836 desktop computer, whose principal means of communication with the ESI will be through an Emulator Interface Circuit Card Assembly (CCA).

The design of the Emulator CCA is a substantial task and is now underway. This Technical Report discusses the design requirements for that CCA and will, we hope, impart some overall understanding of the PSAT Emulator.

It should also be noted that BB&N is producing a new message processor, the BSAT, which streamlines message handling protocols for improved channel throughput. The BSAT will require a substantially revised PSAT/Modem Interface CCA within the ESI Interface Control and Codec Unit. By designing an appropriate BSAT Emulator Interface CCA and revising the HP9836 software, the PSAT Emulator can be updated to a BSAT Emulator without incurring the cost of a totally new design.

M/A-COM LINKABIT, Inc.
10453 Roselle Street
San Diego, CA 92121

EMULATOR INTERFACE CCA

DR. ROBERT MEANS

21 October 1982

Table of Contents

List of Figures

HP/ESI INTERFACE CCA

1. Introduction

The Emulator Interface CCA controls the flow of information between the HP9836 and the ESI. It does this primarily by regulating DMA transfers between the processor CCA's in the PSAT Emulator. Other functions such as Bit Error Rate (BER) measurement, timing of transmitted and received bursts, and Cyclic Redundancy Check calculations are also done on the Emulator Interface CCA.

2. Module Descriptions

Figure 2.1 is a block diagram of the Emulator Interface CCA with the primary modules shown. Each module is explained in more detail in the following sections.

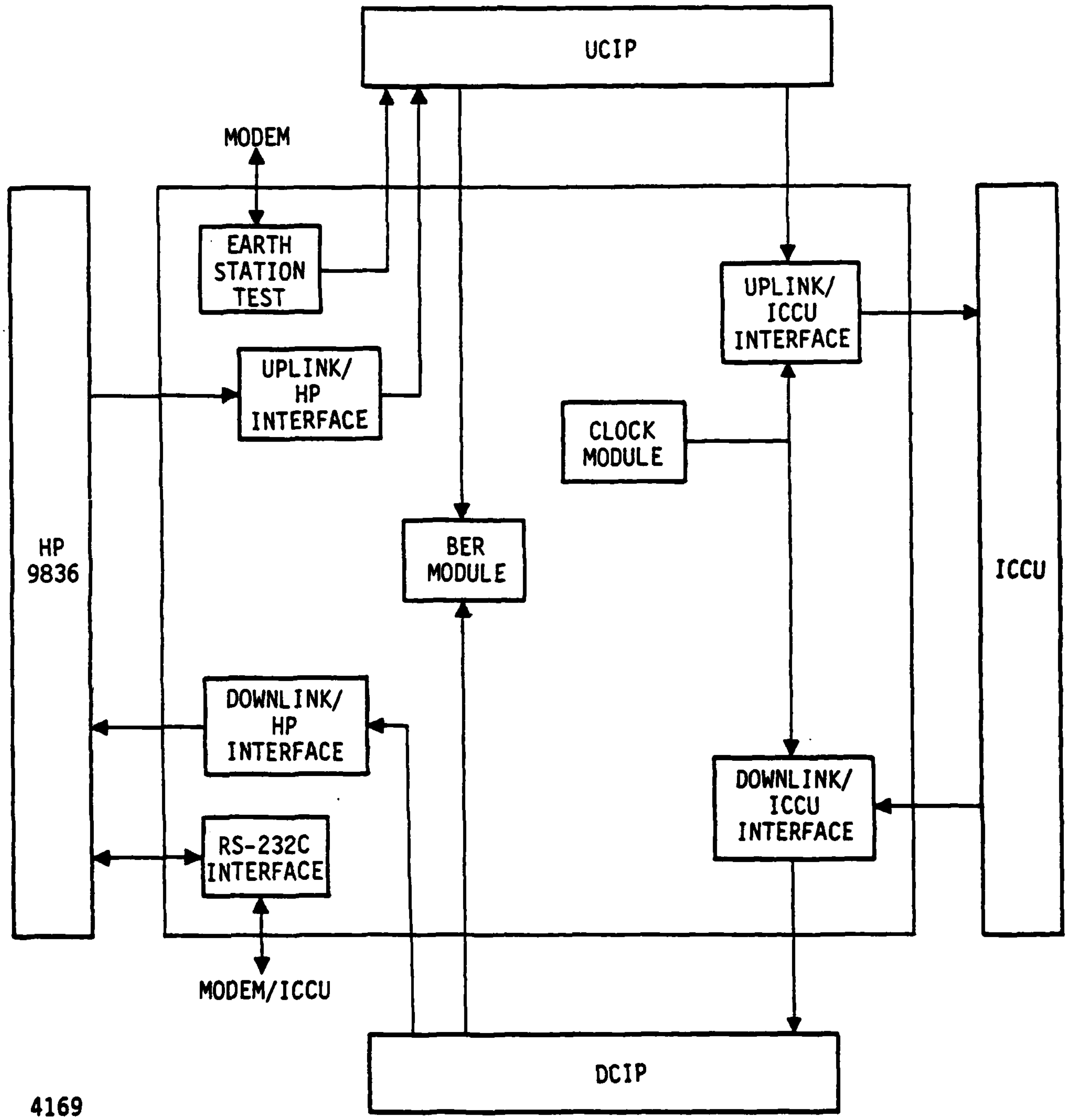
The signals to and from the Emulator Interface CCA are constrained by the fact that the UCIP and DCIP edge connectors signals are almost completely defined for functions necessary for the ICCU. Fortunately many of the same functions are required in the Emulator Interface. However care must be taken to restrict the number of DMA channels to four per board. The number of addressable ports is also limited.

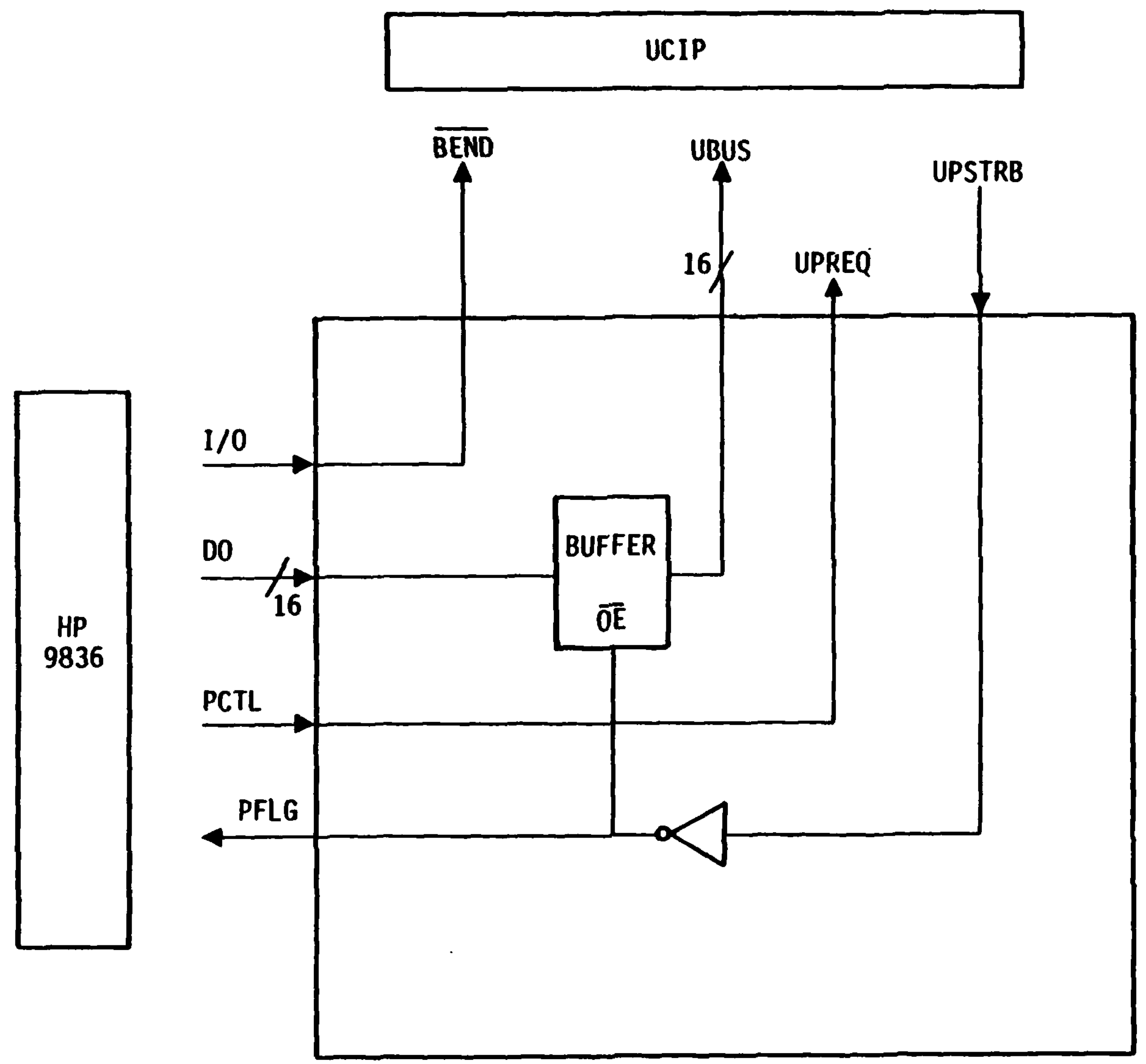
2.1. Uplink/HP Interface Module

The Uplink/HP Interface Module supports communication between the HP9836 and the Uplink CIP. This communication is accomplished via the following signals as shown in Figure 2.2.

DO0-15	UBUS0-15
I/O	BEND
PCTL	UPREQ
PFLG	UPSTRB

Figure 2-1. Emulator Interface CCA Block Diagram





4170

Figure 2-2. Uplink/HP9836 Interface Module

Data is transferred from the HP9836 using the GPIO Interface. This transfer is explained fully in the HP98622A GPIO Interface Manual and the Pascal Procedure Library User's Manual.

DO0-15 is the data bus used to send data from the HP9836.

I/O is generated by the HP9836 and is used to indicate the direction of data transfer. Input is high; output is low.

PCTL is a peripheral control signal generated by the HP9836 and is used to indicate that data is valid on the Bus DO.

PFLG is a peripheral flag signal generated by the Uplink HP Interface. It is driven high to acknowledge PCTL and is driven low to indicate transfer complete.

UBUS0-15 is the data bus of the Uplink CIP.

BEND is generated by the HP9836 I/O signal used to indicate the end of a burst of data from the HP9836.

UPREQ is generated by the HP9836 PCTL and is used for the DREQ of a DMA Transfer device on the Uplink CIP.

UPSTRB is a DACK signal generated by the Uplink CIP DMA Transfer device and is used to create PFLG.

Figure 2.3 shows a timing diagram of the Full Mode Output of a GPIO DMA transfer. Figure 2.4 shows the timing for a Full Mode Input Ready Source GPIO DMA transfer.

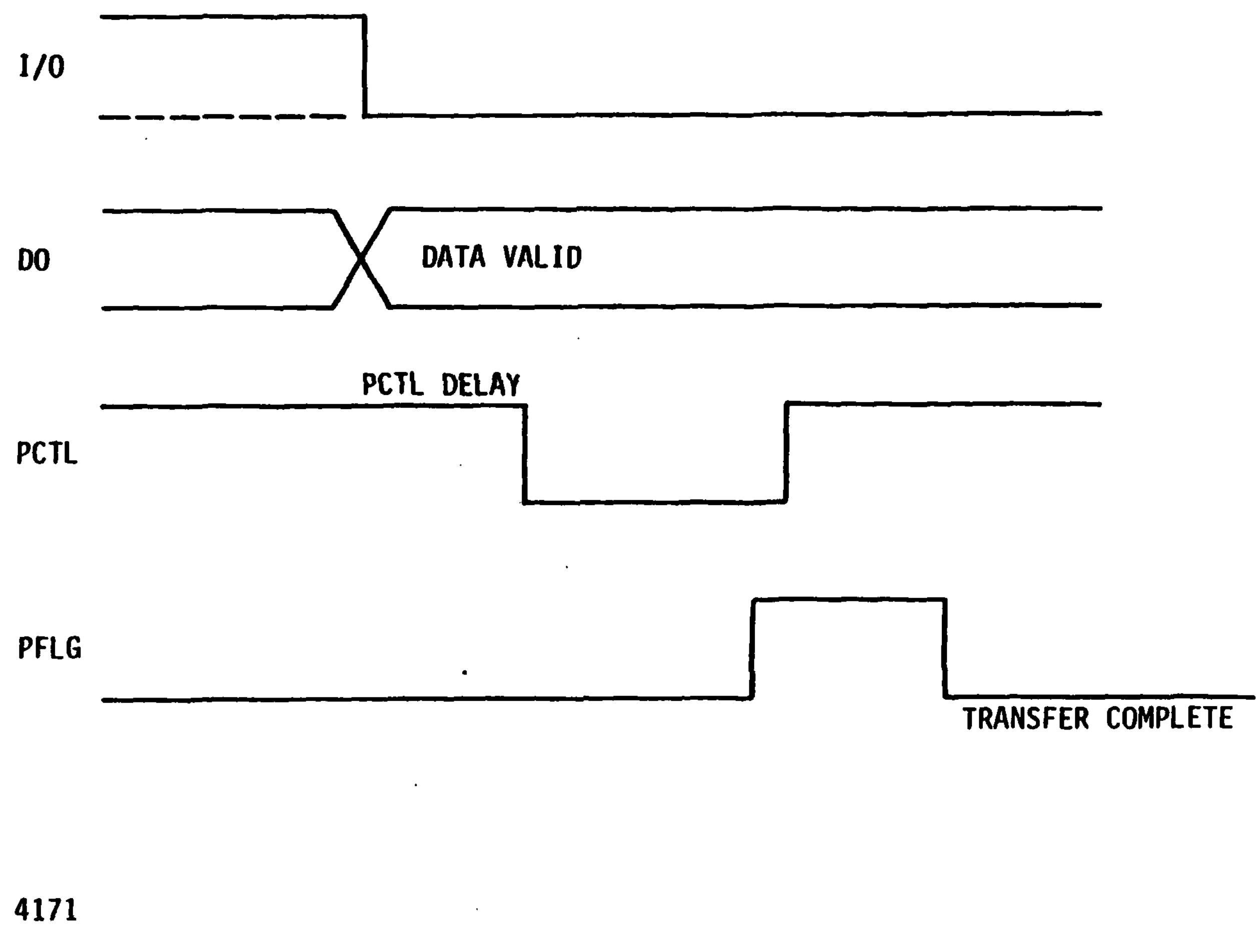


Figure 2-3. Full Mode Output

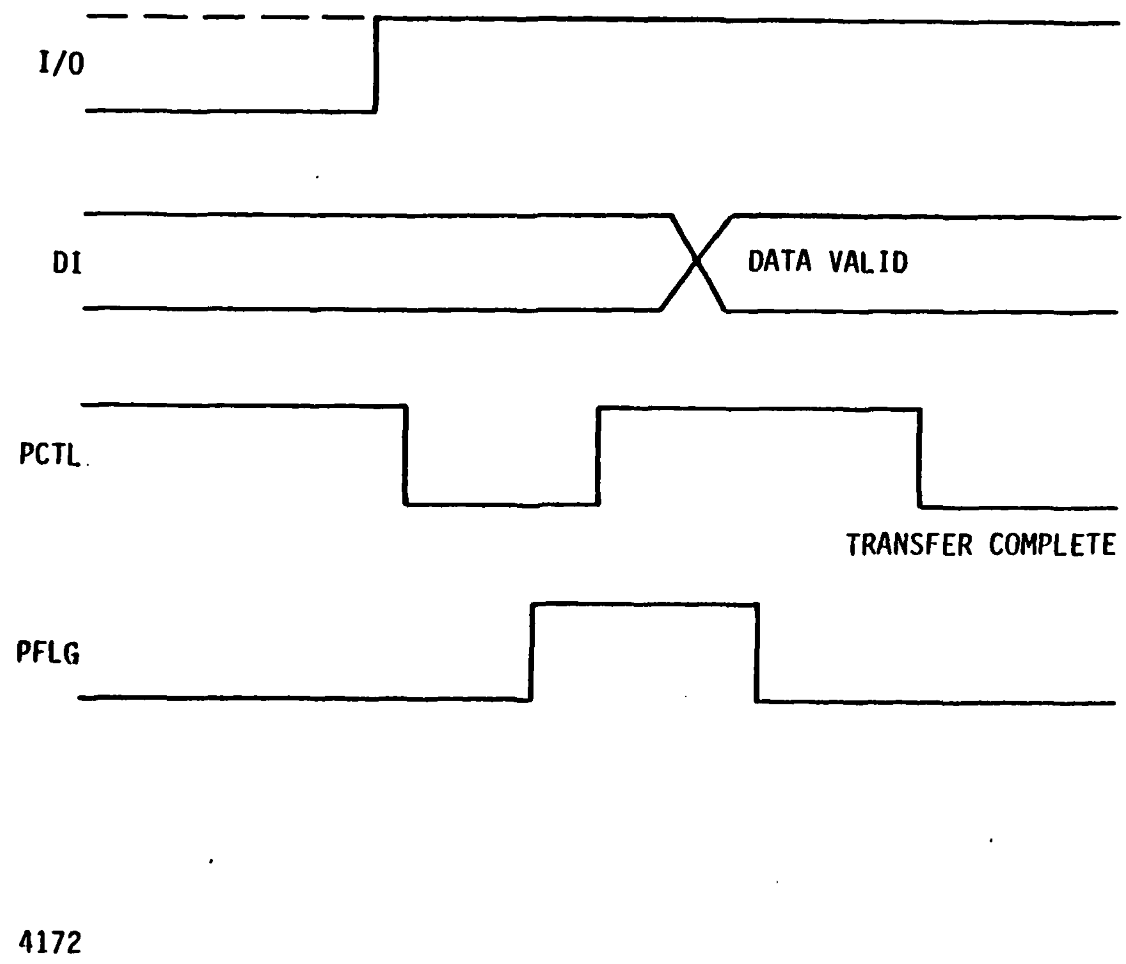


Figure 2-4. Full Input Ready Source

2.2. Uplink/ICCU Interface Module

The Uplink/ICCU Interface Module supports communication between the Uplink CIP and the ICCU. Bursts are sent to the ICCU in such a way as to emulate the PSAT. The transfer is accomplished by the following signals as shown in Figure 2.5.

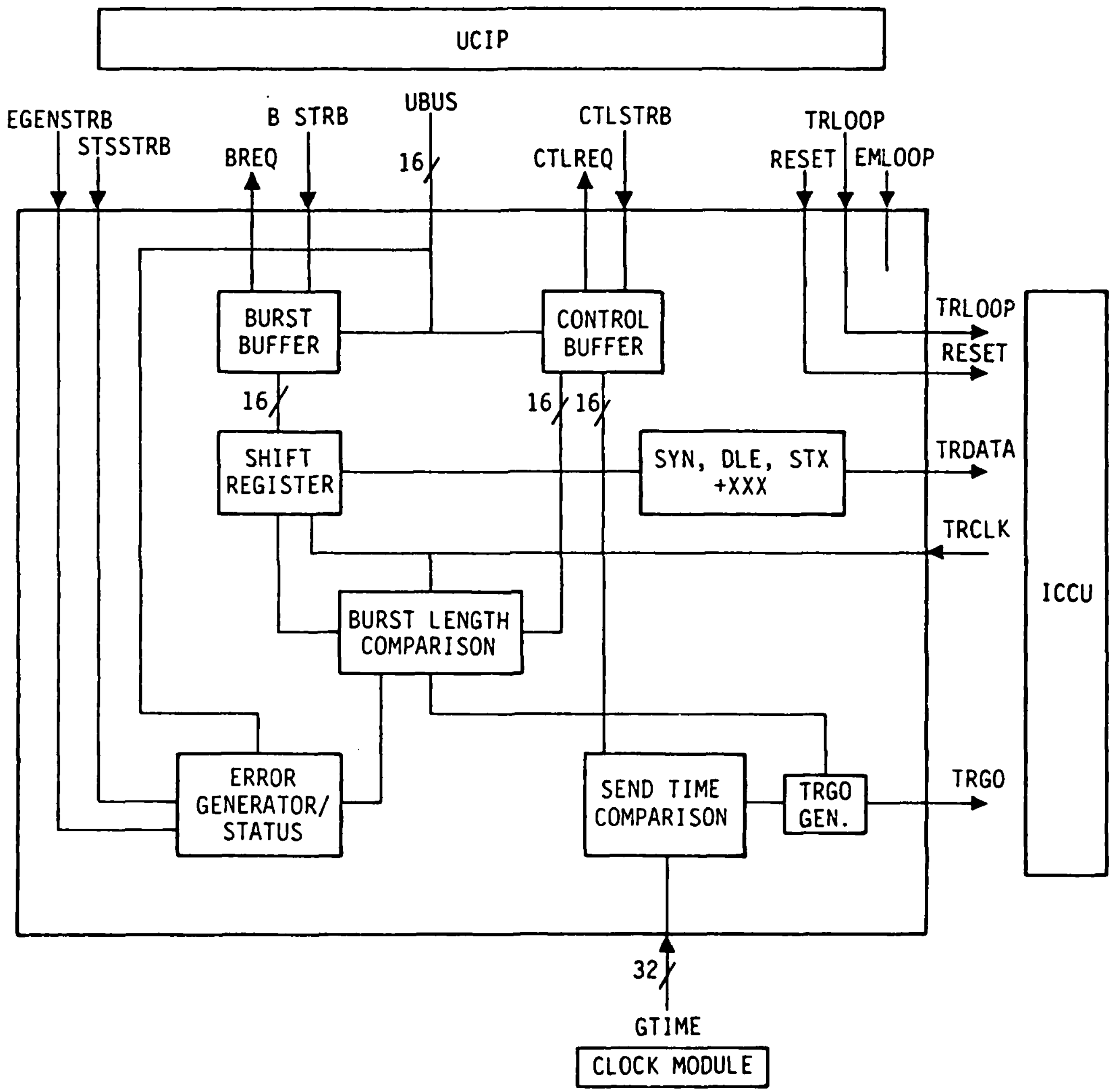
UBUS 0-15	TRGO
BREQ	TRDATA
CTLREQ	TRCLK
BSTRB	GTIME
CTLSTRB	TRLOOP
EMLOOP	RESET

Data is transferred to the ICCU interface in bursts. A burst is a group of less than 4096 16 bit words.

Each burst has three control words associated with it which are sent to a separate buffer. The first word is the burst length (in 16 bit words). The second and third words are the Send Time (32 bits). The burst buffer is filled and the first word loaded into the output shift register. There it lengths and the Send Times are stored in the control FIFO. The Send Time of the first burst is compared to the Global Time. When they are equal, TRGO is asserted, the SYN, DLE, STX preamble is added and data is shifted out of the output shift register by TRCLK. Data is continuously shifted out by TRCLK until a complete burst has been sent. This condition is determined by the comparison of the burst length control word and a count of TRCLK divided by 16. When these are equal 8 bits of filler are appended, TRGO is unasserted and the transfer of words from the burst buffer is halted.

We must be able to generate and recognize error conditions such as TRGO dropping early and not receiving a TRCLK. Status

Figure 2-5. Uplink/ICCU Interface Module



4173

and errors must be communicated to the UCIP. This will be accomplished by the Error Generator/Status Module. The UCIP will communicate the status to the DCIP via the IPC.

UBUS0-15 is the uplink data bus and is used to send burst data and control information to the Uplink ICCU Interface buffers.

BREQ is generated by the Uplink ICCU Interface and is a request to the Uplink CIP DMA for another burst data word.

CTLREQ is generated by the Uplink ICCU Interface and is a request to the Uplink CIP DMA for another burst control word.

BSTRB is generated by the Uplink CIP and is used to latch data into the Uplink ICCU Interface.

CTLSTRB is generated by the Uplink CIP and is used to latch control words into the Uplink ICCU Interface control buffer.

EMLOOP is generated by the UCIP and is used to switch TRDATA, TRCLK, TRGO to RECDATA, RECCLK and RECGO in order to implement the PSAT Emulator loopback.

TRDATA is generated by the Uplink ICCU Interface and carries the data bits to the ICCU.

TRCLK is the 3.088 MHz gated clock generated by the ICCU.

TRGO is a request generated by the Uplink ICCU Interface to send data to the ICCU.

GTIME is the Global Time (32 bits) generated by the Clock Module.

TRLOOP is generated by the UCIP to enable loopback in the ICCU.

RESET is generated by the UCIP to reset the ESI.

2.3. Downlink/ICCU Interface Module

The Downlink/ICCU Interface Module supports communication between the ICCU and the Downlink CIP. The serial RECDATA passes through a CRC Calculation module described in section 2.9 but is essentially unchanged. The communication is accomplished by the following signals as shown in Figure 2.6.

RECDATA	DBUS0-15
RECCLK	DSTRB
RECGO	DREQ
GTIME	DBDONE

A burst is transferred from the ICCU by means of the serial data line RECDATA. The start of a burst is indicated by asserting RECGO. The serial data is accompanied by a gated clock, RECCLK.

A CRC calculation is performed on the serial data. The data passes through this module unchanged except for the CRC words at the end of the control packet and the CRC words at the end of the data packet. These words are replaced by zero if the CRC words are correct. Otherwise they remain unmodified.

Each received burst is timestamped with the 32 bit Global Time and these two words are stored in the output buffer and are sent to the Downlink CIP as the first two words of the received burst.

RECDATA is generated by the ICCU and carries the data bits to the Downlink ICCU.

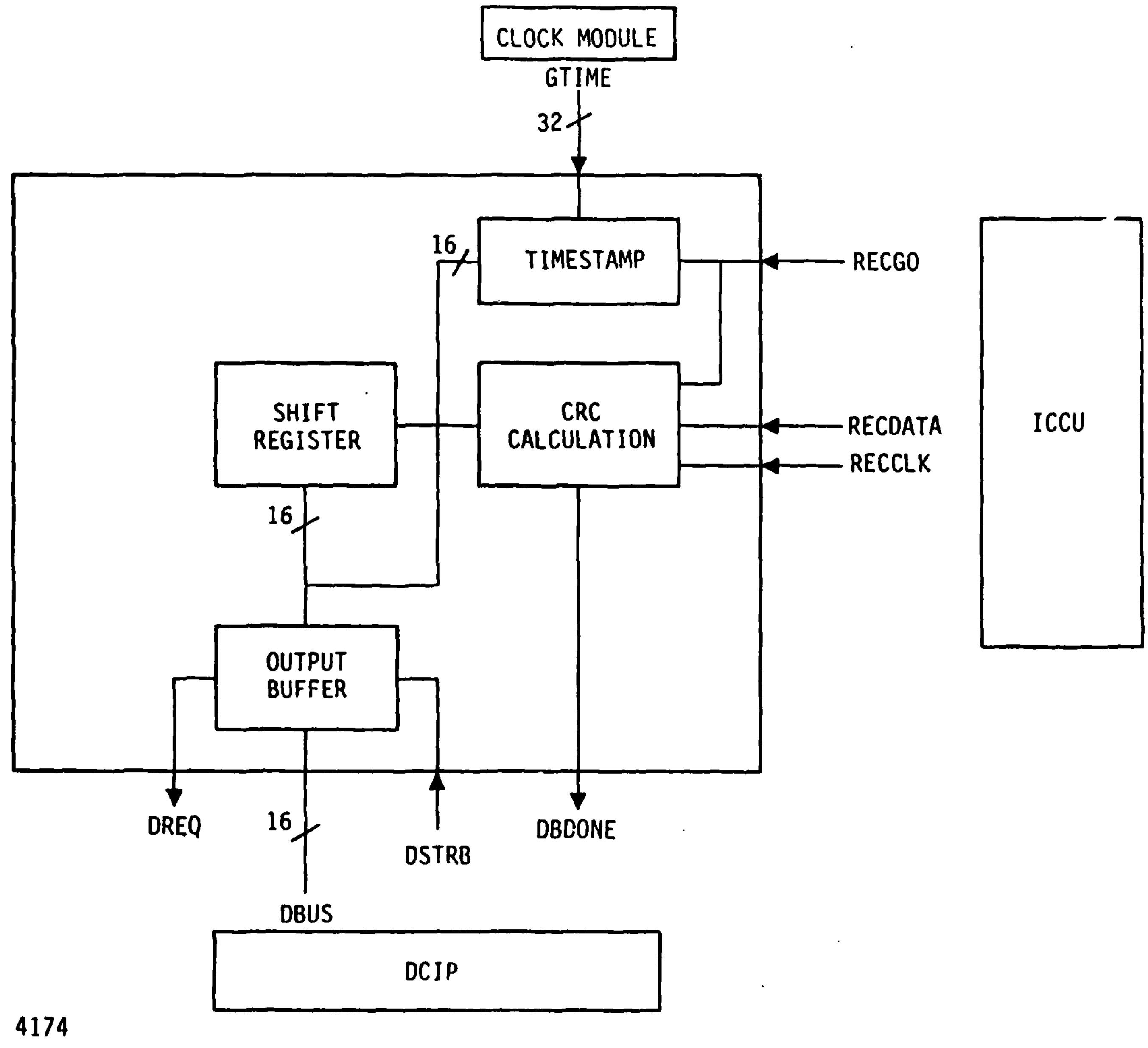


Figure 2-6. Downlink/ICCU Interface Module

RECCLK is the 3.088 MHz clock generated by the ICCU which controls the sampling of the data on the signal line RECDTA.

RECGO is generated by the ICCU and is asserted at the start of the received burst transmission. It remains asserted until the end of the burst transmission.

DBUS0-15 is the Downlink CIP data bus.

DDATASTRB is generated by the Downlink CIP and is used to acknowledge transfer of burst data.

DDATAREQ is generated by the Downlink ICCU Interface and is used to request a transfer of burst data to the Downlink CIP DMA.

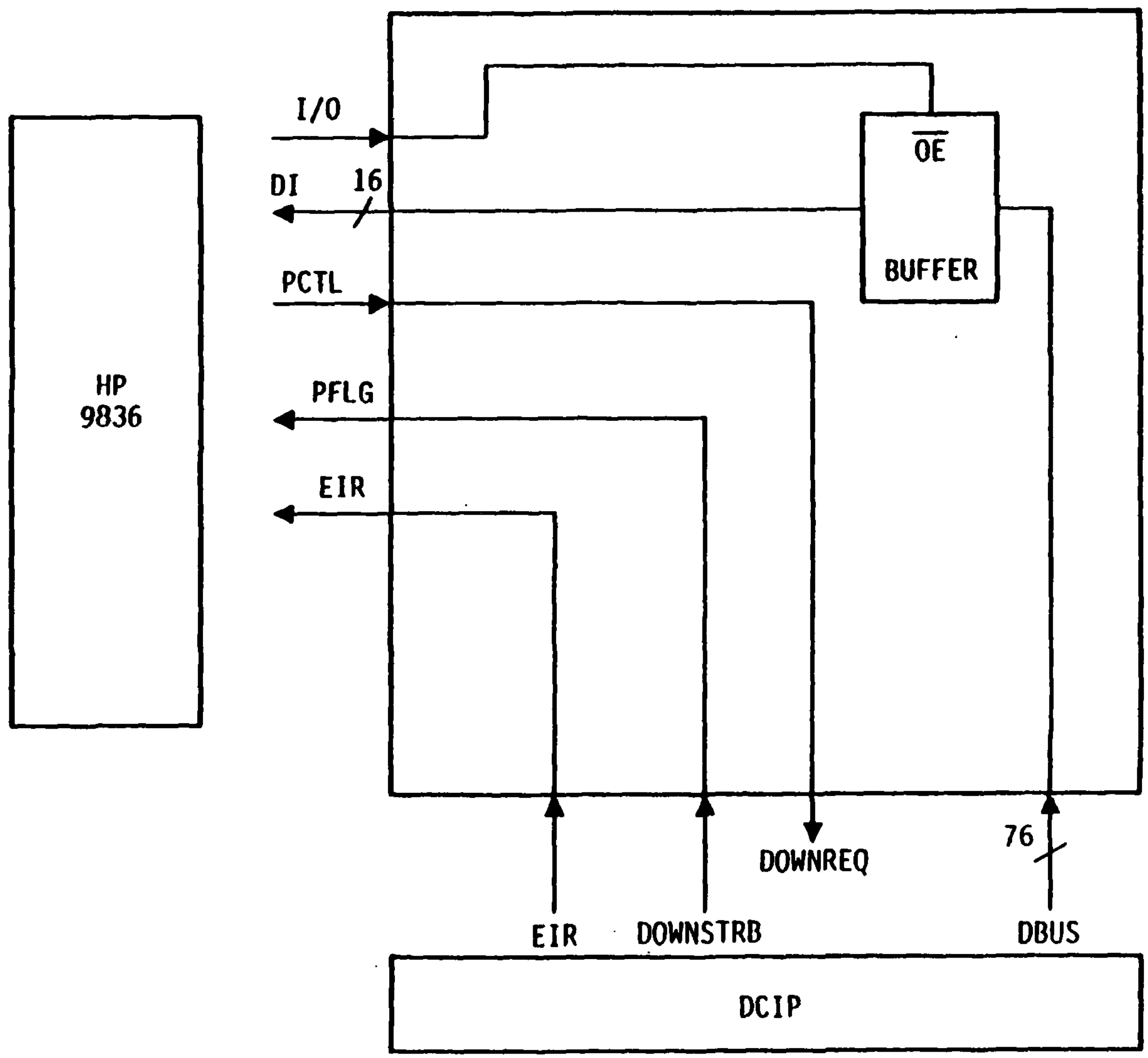
DBDONE is generated by the Downlink ICCU Interface and is used to inform the Downlink CIP DMA that the last word has been transferred.

2.4. Downlink/HP9836 Interface Module

This module supports communication between the HP9836 and the Downlink CIP. This communication is accomplished via the following signals as shown in Figure 2.7.

DBUS0-15	I/O
DOWNREQ	DI0-15
DOWNSTRB	PCTL
EIR	PFLG

Burst data and other information is transferred from the Emulator to the HP9836 by means of a DMA transfer using the GPIO Interface. Such transfers must be set up and controlled by the HP9836 processor. This control can be established by an interrupt request from the Downlink CIP when it is ready to send



4175

Figure 2-7. Downlink/HP9836 Interface

data to the HP9836. The transfer Timing diagram is given in Figure 2.4.

Note that the signals I/O, PCTL and PFLG are also used in the Uplink/HP9836 Interface and must be multiplexed. This is not shown in the block diagram.

DBUS0-15 Is the Downlink CIP data bus and is used to transfer ESI performance information between the PSAT Emulator and the HP9836.

DOWNREQ is a request from the HP9836 for data and asks the Downlink CIP to place data on the data bus.

DOWNSTRB is generated by the Downlink CIP and tells the HP9836 that data is on the data bus.

EIR is an external interrupt from the Downlink CIP to the HP9836 requesting the HP9836 to begin a DMA transfer.

DI0-15 is the data bus used to receive data by the HP9836.

PCTL is a peripheral control signal generated by the HP9836 and is used to request the peripheral to put data onto the data bus and to indicate transfer complete and readiness for the next cycle.

PFLG is a peripheral flag signal generated by the Downlink HP Interface. It is driven high to acknowledge the transfer complete and is driven low to indicate valid.

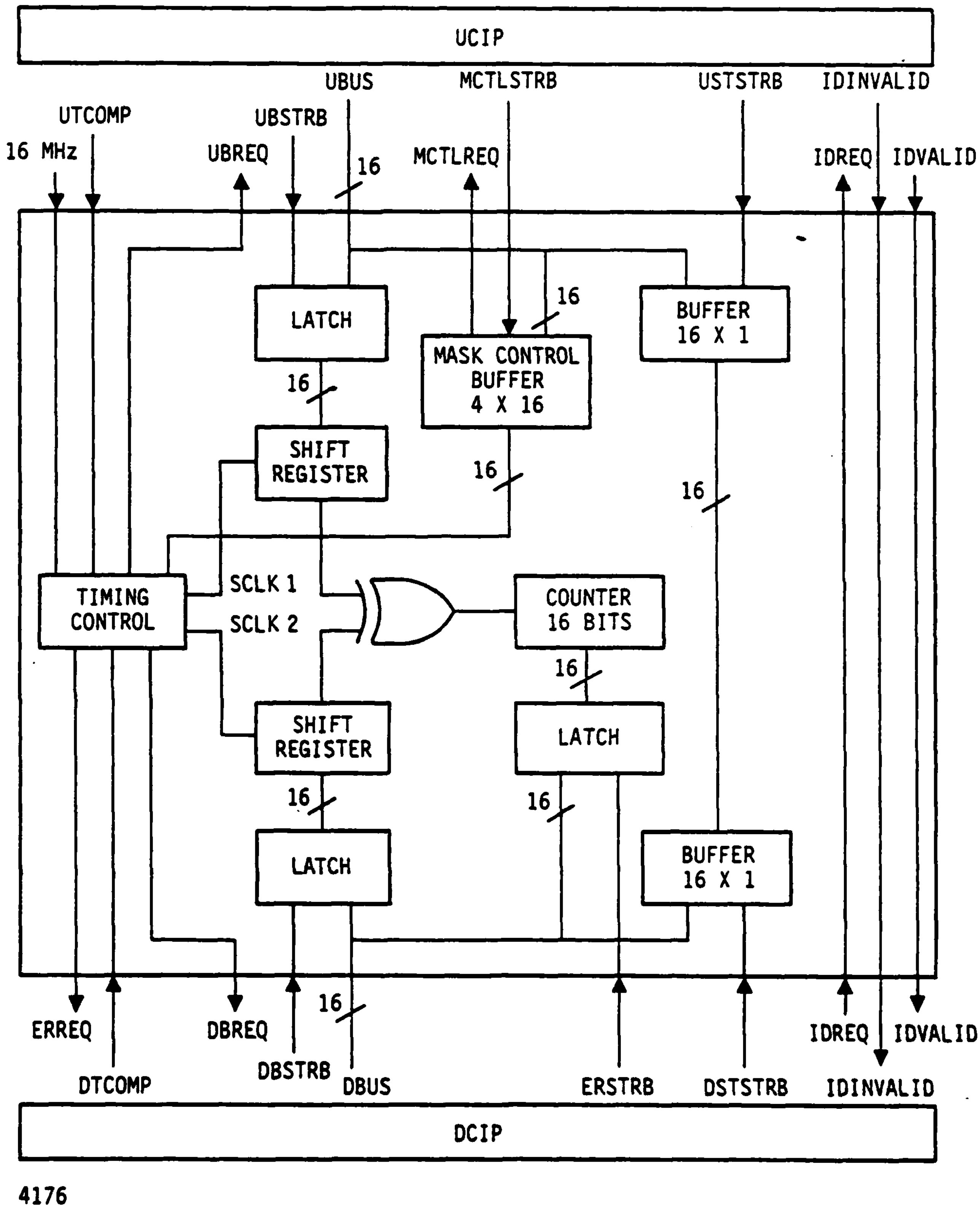
I/O is generated by the HP9836 and is used to indicate direction of data transfer. Input is high; output is low.

2.5. BER Comparison Module

The BER Comparison Module compares a received data burst to the data burst that should have been received. A block diagram is shown in Figure 2.8. A copy of the data burst as it should have been received is stored in the Uplink CIP memory. It is identified by Burst ID. When a data burst is received by the Downlink CIP, it is identified by its Receive Time and Burst ID. The fixed ESI delay plus the Burst Delay Word can be used by the Downlink CIP to generate the received burst's Send Time. A request to the Uplink CIP for a copy of the burst identified by the received burst's Burst ID is sent to the Uplink CIP. The Uplink CIP determines if the Burst ID is valid and, if so, a DMA transfer of the burst is begun to the BER Comparison Module. The Downlink CIP is also notified that the Burst ID was valid. If the Burst Id was invalid then the Uplink CIP notifies the Downlink CIP of that fact. Upon receipt of notice that the Burst ID was valid, the Downlink CIP begins a DMA transfer of the received burst to the BER Comparison Module. Upon receipt of notice that the Send Time was invalid, the Downlink CIP send an appropriate message to the HP9836. The received burst's send time (as calculated by the DCIP) is compared to the scheduled send time which has been sent to the DCIP from the UCIP. The HP9836 is notified of any discrepancy. If all is in order, the bursts are compared and the number of errors is transferred to the DCIP for later transfer to the HP9836.

The mask control buffer operates in a manner similar to the encoder control word buffer in the ICCU. It will be able to control the counting of bit errors for selected portions of the burst. The burst may be broken down into a maximum of four segments for which error counts will be provided to the DCIP.

Figure 2-8. BER Comparison Module



The Timing Control block will send a separate ERREQ to the DCIP when each error count is ready. The Timing Control block will therefore contain (among other components) a presettable 16 bit counter to control the error count and a counter to count SCLK (=8 MHZ) which will clock out 16 bits from the data shift register and then request another burst data word.

The BER Comparison Module uses the following signals:

DBUS0-15	UBUS0-15
DTCOMP	UTCOMP
DBREQ	UBREQ
DBSTRB	UBSTRB
ERSTRB	16 MHZ
DSTSTRB	USTSTRB
STREQ	IDVALID
ERREQ	IDINVALID

DBUS0-15 is the Downlink data bus and is used to transfer burst data, Send Times, and bit error counts.

DTCOMP is generated by the Downlink CIP and is used to indicate that a burst transfer is complete.

DBREQ is generated by the BER Comparison Module and is a request to the Downlink CIP DMA for another burst data word.

DBSTRB is generated by the Downlink CIP and is used to latch burst data into the BER Comparison Module downlink buffer.

ERSTRB is generated by the Downlink CIP and is used to read the Bit Error Count.

ERREQ is generated by the BER Comparison Module and is used to notify the Downlink CIP that the Bit Error Count is available.

DSTSTRB is generated by the Downlink CIP and is used to latch the Send Time into the BER Comparison Module.

STREQ is generated by the Downlink CIP and is used to notify the Uplink CIP that a copy of a burst is requested.

UBUS0-15 is the Uplink CIP data bus and is used to transfer burst data and Send Times.

UTCOMP is generated by the Uplink CIP and is used to indicate that a burst transfer is complete.

UBREQ is generated by the BER Comparison Module and is a request to the Uplink CIP DMA for another burst data word.

UBSTRB is generated by the Uplink CIP and is used to latch burst data into the BER Comparison Module uplink buffer.

16 MHZ is generated by the Uplink CIP and is used to generate timing and clocks for the BER Comparison Module.

USTSTRB is generated by the Uplink CIP and is used to read the Send Time from the BER Comparison Module after having received a STREQ.

IDVALID is generated by the Uplink CIP and is used to notify the Downlink CIP that the Burst ID was valid.

IDINVALID is generated by the Uplink CIP and is used to notify the Downlink CIP that the Burst ID was invalid.

The correct identification of a burst is essential in this scheme in order to be able to compare the burst for transmission errors. A precise knowledge of the ESI round trip time is useful. This time can be measured by the PSAT Emulator by means of a burst every 8 frames. This is controlled by the software, but is mentioned here to point out that even transmissions over the satellite channel may be accommodated by this normalization method. It may be necessary to allow a window of GTIME clocks for a valid comparison in order to allow for satellite round trip time variations.

2.6. Clock Module

The Clock Module supplies a 32 bit global time clock to other modules which need it. These modules are the Uplink/ICCU Interface and the Downlink/ICCU Interface. The clock consists of a 32 bit counter driven by LTCLOCK which is usually supplied by the ICCU. If the ICCU is not present (as in PSAT Emulator loopback tests) the Clock module must be able to generate its own LTCLOCK from the 16 MHZ clock from the UCIP. The Clock Module is shown in Figure 2.9. Its functions are accomplished by the following signals:

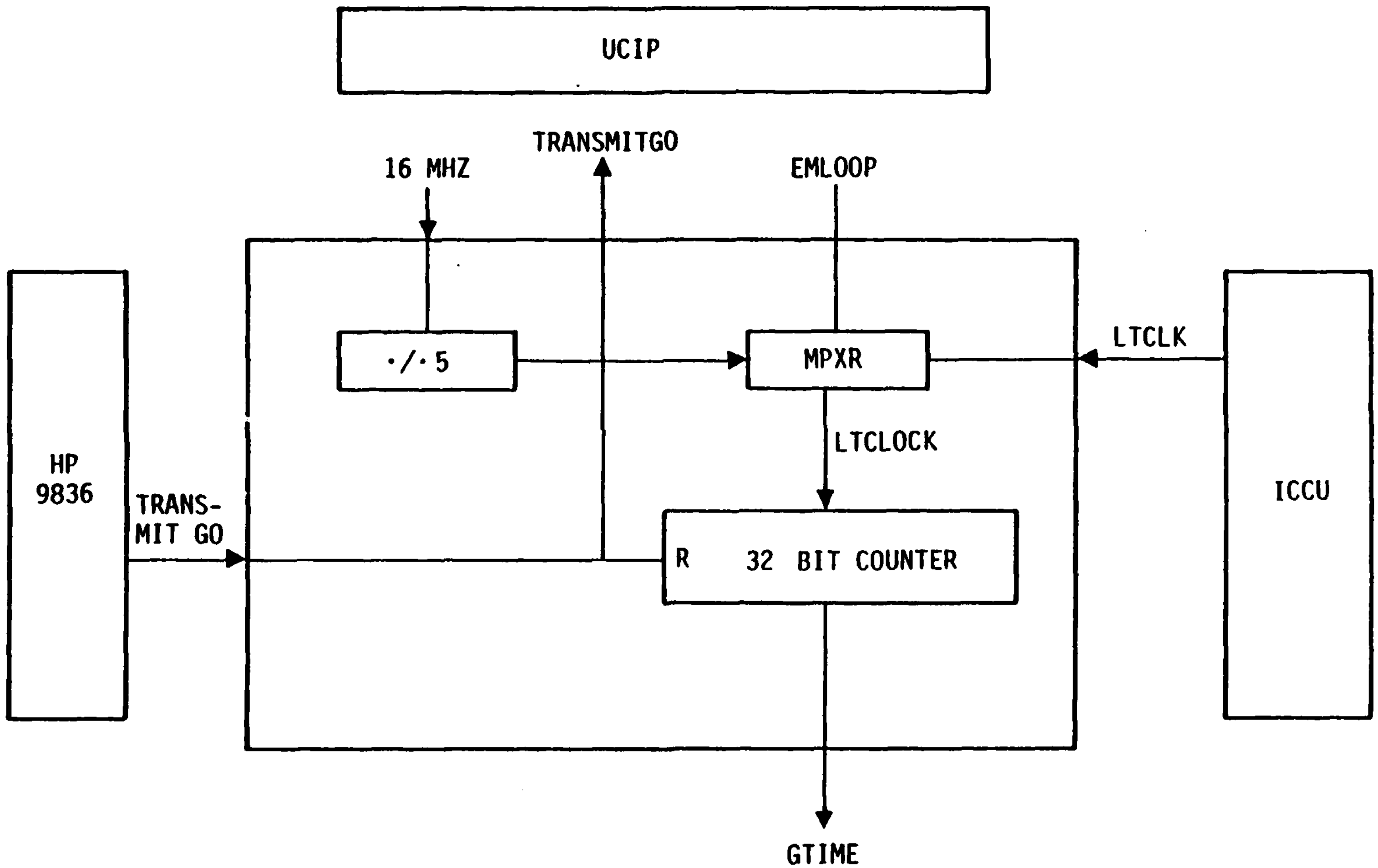
16 MHz	GTIME0-32
LTCLK	TRANSMITGO
CRESET	

<u>16MHZ</u> is generated by the Uplink CIP and is used to generate an internal LTCLOCK.

<u>LTCLK</u> is generated by the ICCU and is used to generate LTCLOCK when the ICCU is present.

<u>CRESET</u> is generated by the UCIP and is used to reset the Global Time counters.

<u>GTIME0-32</u> is a 32 bit count of LTCLOCK which will cycle



4177

Figure 2-9. RS-232C Switch Module

approximately every 23 minutes.

EMLOOP is generated by the UCIP in order to control the source of LTCLOCK when the PSAT Emulator is in a loopback test.

TRANSMITGO is generated by the HP9836 GPIO Interface and is used to reset the clock.

2.7. RS-232C Switch Module

The RS-232C Switch Module controls the serial communication link between the HP9836 and the ESI. The HP9836 will be allowed to communicate with either the ICCU or the HSBM. The HP9836 generated signal CTL1 will be used to switch the two ports. A relay should be used to implement the switch in order to avoid voltage translation problems which would require another power supply in the PSAT Emulator. The switching is accomplished as shown in Figure 2.10 using the following signals.

CTL1	RXICCU
TXD	RXHSBM
RXD	TXICCU
RTS	RXHSBM
CTS	
DSR	
DTR	

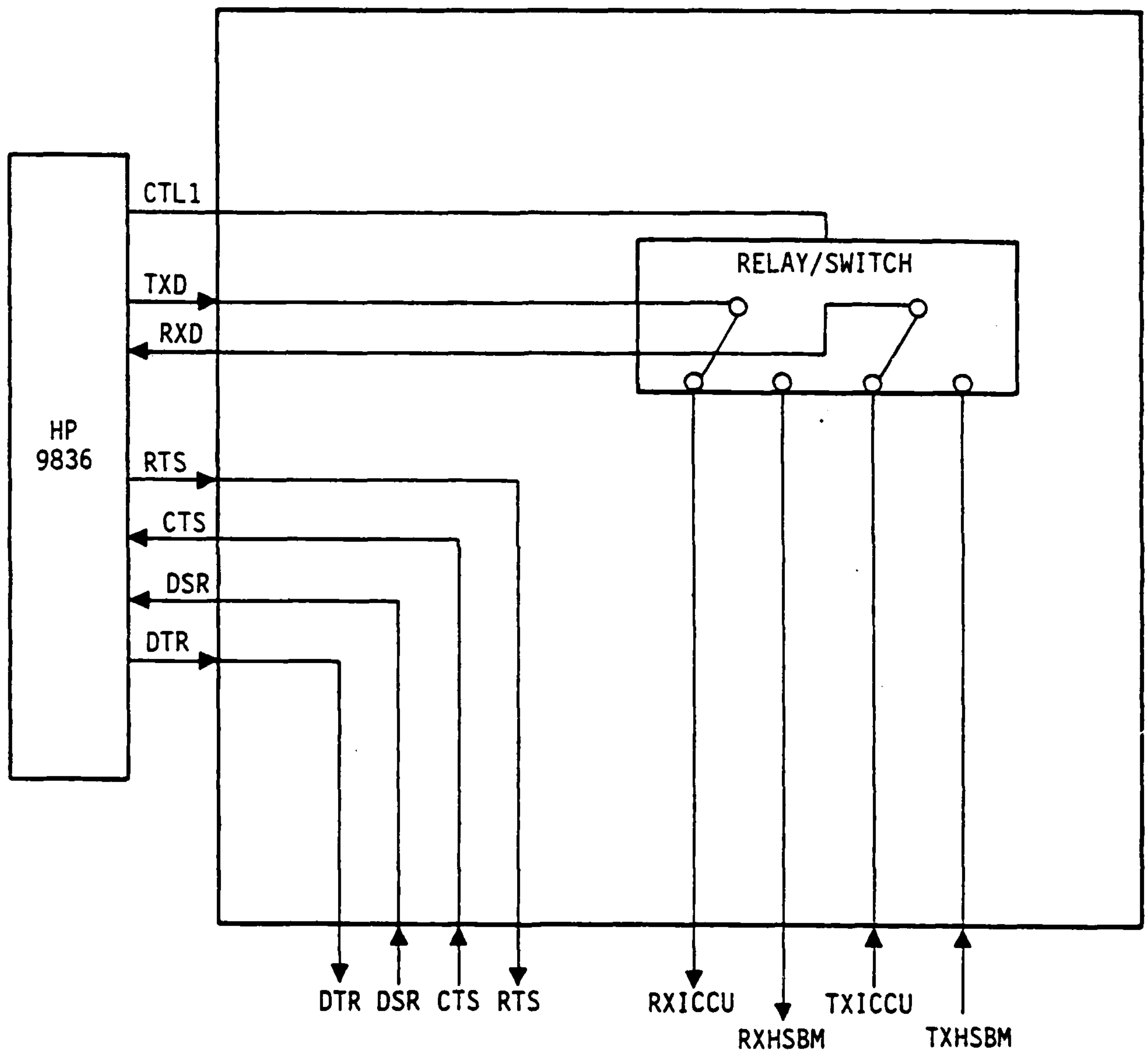
CTL1 is part of the GPIO interface and is generated by the HP9836. It will switch the communication path between the ICCU and the HSBM.

TXD is the transmitted data from the HP9836.

RXD is the received data from the ICCU or HSBM.

RTS is a request to send from the HP9836.

Figure 2-10. Earth Station Test Module



4178

CTS is a clear to send signal from the ICCU or HSBM.

DSR is a data set ready signal generated by the ICCU or HSBM indicating to the HP9836 that the power is on.

DTR is a data terminal ready from the HP9836 and indicates that the HP9836 is ready to transmit or receive data.

RXICCU is the received data from the standpoint of the ICCU.

RXHSBM is the received data from the standpoint of the HSBM.

TXICCU is the transmitted data from the ICCU.

TXHSBM is the transmitted data from the HSBM.

The signals DTR, DSR, CTS and RTS go both to the HSBM and ICCU. This is not explicit in the block diagram. The relay/switch module which switches between the ICCU and HSBM must have a break before make type of action so that the ICCU and HSBM are not both connected at the same time. This is a Type C SPDT relay.

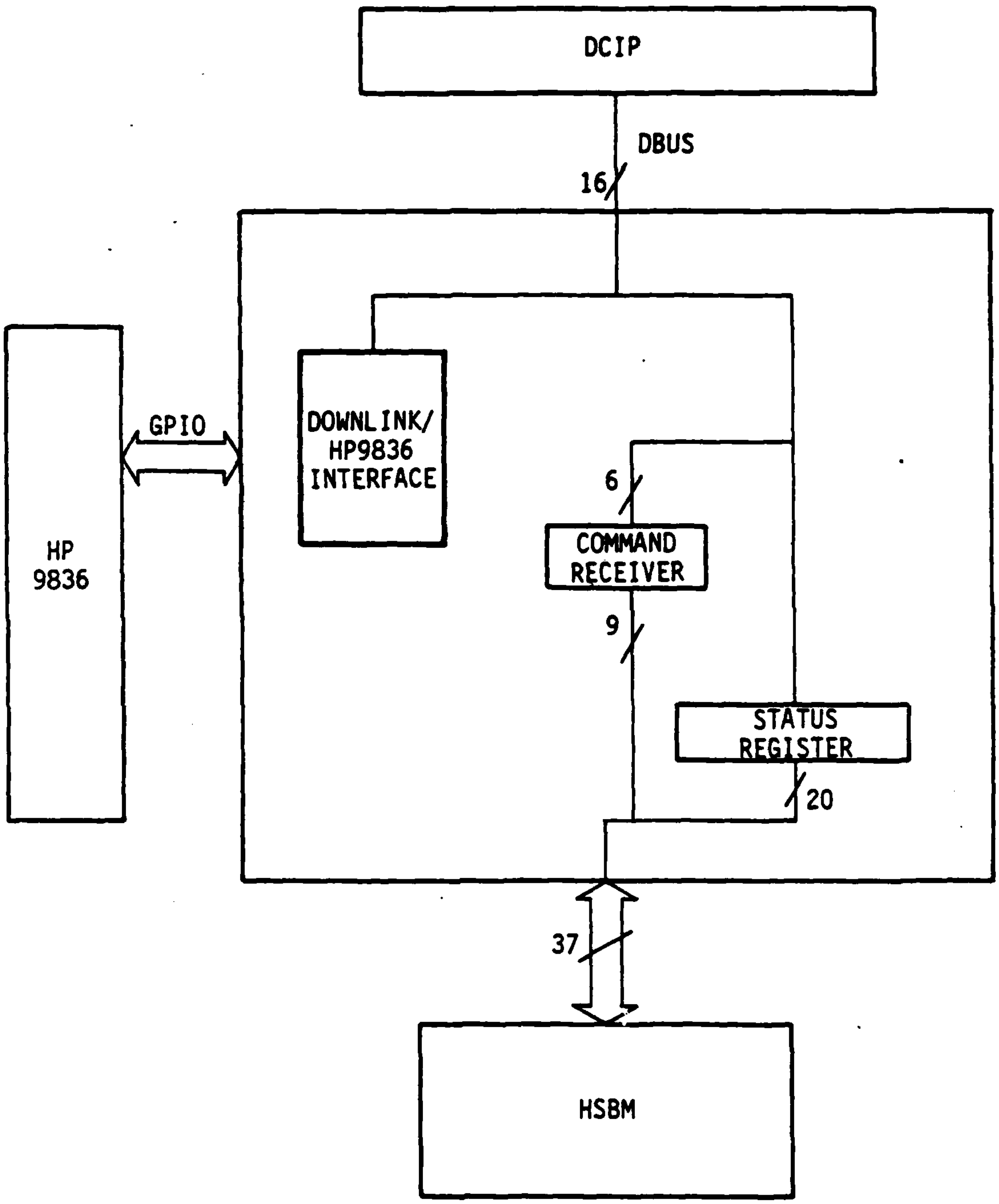
2.8. Earth Station Test Module

The Earth Station Test Module is used to test and verify the correct operation of all commands generated by the HSBM to control and monitor the Earth Station. In order to avoid the necessity of the Uplink CIP communicating with the Downlink CIP, the HSBM will initiate the test after being commanded to do so by the RS-232C communication link.

The test itself will be conducted by the Downlink CIP and the

HSBM with the results communicated to the HP9836 by the GPIO Interface. The Earth Station Test Module is shown in Figure 2.11. Its uses the signals as specified in Table 2.1. Note that these signals are divided into two groups: status and command.

Figure 2-11. Earth Station Test Module



4179

Table 2-1. LBM36A/Earth Station Signals

Connector	Signal	Description
1	Up Converter Fail	Status
2	Power Supply Fail	Status
3	Low Temperature Alarm	Status
4	HPA Fail	Status
5	GND	
6	Tx on/off	Status
7	Test Translator Fail	Status
8	RF Loop On	Command that initiates a carrier loopback at the RF point in the Earth Station
9	RF Loop Off	Command that disables an existing RF loopback condition within the Earth Station.
10	GND	
11	HPA Power Bit 0	Status
12	HPA Power Bit 2	Status
13	HPA Power Bit 4	Status
14	HPA Power Bit 6	Status
15	GND	
16	IF Loopback	Status
17	GND	
18	RF Loopback	Status
19	GND	
20	Down Converter Fail	Status
21	Over Temperature Alarm	Status
22	Intrusion Alarm	Status
23	LNA Fail	Status
24	GND	
25	TX Enable	Command that turns on the Earth Station HPA.
26	IF Loop On	Command that initiates a carrier loopback at the IF point in the Earth Station
27	IF Loop Off	Command that disables an existing RF loopback condition within the Earth Station.
28	TX Disable	Command that turns off the Earth Station HPA.

Table 2-1. LBM36A/Earth Station Signals Continued

Connector	Signal	Description
29	COMMAND RETURN*	
30	HPA Power Bit 1	Status
31	HPA Power Bit 3	Status
32	HPA Power Bit 5	Status
33	HPA Power Bit 7	Status
34	GND	
35	GND	
36	COMMAND RETURN*	
37	COMMAND RETURN*	

*The COMMAND RETURN lines are provided as the common return paths for the six command lines (TX Enable, etc.). These are isolated from GND and are connected to one contact of each of the six command relays.

There are twenty status signals that the HP9836 must define. Except for the HPA power bits, which consists of an 8 bit word proportional to the microwave amplifier output power, the status bits are active low. A low signal indicates a false, off or abnormal condition. The six commands are generated by the HSBM and consist of relay closures of at least 250 ms to the command ground lines for a specified closure time. A line receiver such as a 26LS32 could be used to receive them. The DCIP must measure the compliance of the HSBM to these pulse duration requirements and generate appropriate status bits for the HSBM to read. The PSAT Emulator reports the results of its test to the HP9836 via the GPIO Interface. The HSBM reports the result of its tests to the HP9836 via the RS-232C Interface. Figure 2.11 doe not shown the strobes, requests and interrupts. This test module, since it must coordinate software between the HP9836, DCIP and HSBM is not yet fully defined.

2.9. CRC Calculation Module

The CRC Calculation Module is a block inside the Downlink/ICCU Interface Module. A 32 bit Cyclic Redundancy Check (CRC) checksum is used for error detection on all bursts sent by the PSAT. There is one appended to each control packet and to each data packet. The polynomial used to generate the CRC is $x^{32} + x^{22} + x^{2} + x + 1$. The generation circuitry is identical to that used in the ICCU PSAT/Modem Interface CCA. The control circuitry for the checksum generation must be able to compute the checksum for only the control packet. This is simpler than the control required for the PSAT/Modem Interface CCA. The inputs and outputs of this module are shown in Figure 2.6. The SYN DLE STX should be stripped from the burst before being sent to the output shift register.

2.10. BSAT Compatibility

The BSAT will use HDLC protocol on bursts sent and received from the ESI. At present the interface consists of two serial ports, each capable of running at 2 MHz. A new Emulator Interface CCA would be required to support the BSAT. The Uplink CIP and Downlink CIP would remain the same. The changes envisioned to the Emulator Interface would be minor since the HDLC error and flow control will not be used initially.